A CMOS Fully-Integrated Wireless Power Receiver for Autonomous Implanted Devices

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***Abstract*—In this paper we present the design of a wireless power receiver fully integrated. The circuit was constrained to occupy a silicon area of 1.5 $mm \times$ 1.5 mm in a 0.18 μm RF-CMOS process. The main target was to optimize the part of the power transfer efficiency concerning only the receiver side. In that way, we optimized the quality factor of the integrated inductor, the impedance matching conditions and the rectifier efficiency. The simulated quality factor of the integrated inductor was 22 using a link frequency of 1 GHz. Post-layout simulations of the entire system shows that the combined efficiency of the impedance matching network and the rectifier is 57% when the available power at the inductor is 1 dBm. Moreover, the system uses backscattering to respond to the transmitter, allowing to infer the total power transfer efficiency.**

I. Introduction

There is a growing interest in the use of electronic implanted devices for applications such as sensor networks, medical systems and remote instrumentation. These applications have in common the demand for miniaturized and autonomous devices, with difficult or even no access for energy source replacement. In this context, the batteries are unsuitable and the energy must be supplied by means of wireless power transferring (WPT) [1]. Two magnetically coupled inductors are usually employed for wireless power transferring, one of them is packaged together with the embedded electronic circuit. The on-chip integration of the receiving inductor must be pursued in order to reduce size and cost, to increase mechanical robustness and to achieve mass production.

While inductive links implemented with printed boards have been widely studied [2–4], the integration of the WPT system in a single silicon die is rare. In [2], the authors explore the design of inductive links for powering implants in several scenarios, including the effect of biological tissue and considering the possibility of using an integrated inductor in a CMOS process, but they did not implement a full receiver. The implementation of a complete WPT system, operating at 1 GHz, was reported in [5], nevertheless the inductors are out of the chip. The efficiency of the 3-stage rectifier was 65%, however, the losses on the matching network were not taken into account. A rectifier presenting 86% of efficiency was brought in [6]. Nonetheless, they designed a single-stage circuit, that is difficult to match with simple networks and requires a high-voltage amplitude signal at the input. The theoretical work discussed in [7] suggest that the optimal frequency for powering implants is in the GHz scale, without considering that the frequency where occurs the maximum quality factor of an inductor depends on its size and on the number of turns. In [8], a matching network was proposed using an additional inductor which would not be a good option in an integrated system because of the poor quality factor of on-chip inductors.

The main objective of this work is to demonstrate the possibility of a wireless power receiver fully integrated, constrained to an area of 1.5 $mm \times$ 1.5 mm in the IBM 0.18 μm CMOS process. The energy is received on-chip via an inductive link. To achieve this goal, an inductor occupying the outermost area of the chip was integrated. The chip also includes the impedance matching, the voltage rectifier and a circuit that functions as variable load for the receiver and at the same time generates a response, which will be communicated to the transmitter using the same inductive link.

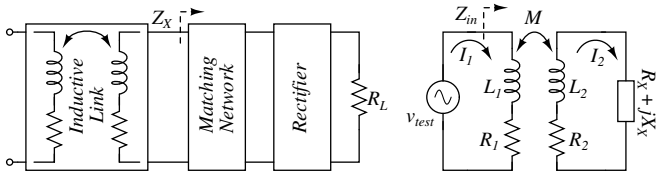


Fig. 1. (a) WPT system. (b) Inductive link model.

II. Wireless Power Transfer Efficiency

The WPT system is responsible to receive and process the energy delivered to the implanted device. As shown in Fig. 1(a), it is composed of an inductive link, a matching network and a rectifier. The link is formed by two inductors as shown in Fig.1(b). Each inductor $L_{1(2)}$ has a series equivalent resistance $R_{1(2)}$, modeling the losses. M=$k\sqrt{L_1 L_2}$ is the mutual inductance and k is the magnetic coupling factor with values ranging from 0 to 1. The equivalent load impedance is Z_X=R_X+jX_X. The link power efficiency (η_0) is defined as the ratio between the power at the load ($|I_2|^2 R_X$) and the power delivered to the link ($|I_1|^2 \Re e\{Z_{in}\}$), where I_1 and I_2 are the mesh currents and $\Re e\{Z_{in}\}$ is the real part of Z_{in}, the link input impedance. Solving I_1 and I_2 by mesh analysis we obtain:

$$\eta_0 = \frac{(\omega M)^2 R_X}{R_1[(\omega L_2+X_X)^2+(R_2+R_X)^2]+(\omega M)^2(R_2+R_X)}. \quad (1)$$

This function is maximized with respect to X_X, when X_X=$-\omega L_2$. Under this condition, we can calculate the reciprocal of the link efficiency ($1/\eta$) as:

$$\frac{1}{\eta} = \frac{1}{\eta_0}\bigg|_{X_X=-\omega L_2} = \frac{R_1 R_2}{(\omega M)^2}\left(\frac{R_2}{R_X}+2+\frac{R_X}{R_2}\right)+\frac{R_2}{R_X}+1. \quad (2)$$

Recognizing that $\omega L_{1(2)}/R_{1(2)}$ is $Q_{1(2)}$, the quality factor of the primary (secondary) inductor, defining p=R_2/R_X and using (2), we can write the reciprocal of efficiency (η_T) of the WPT system as:

$$\frac{1}{\eta_T} = \frac{1}{\eta_{RT}}\left[\frac{1}{k^2}\frac{1}{Q_1}\frac{1}{Q_2}(p+2+\frac{1}{p})+p+1\right], \quad (3)$$

where η_{RT} was included to account for the rectifier efficiency. The matching network was considered lossless in (3). In this work, we are only concerned with the implanted part of the WPT system, then, the product $\frac{1}{k^2}\frac{1}{Q_1}$ is considered as an input parameter. Moreover, we assume that the link is weakly coupled, since it is the worst case

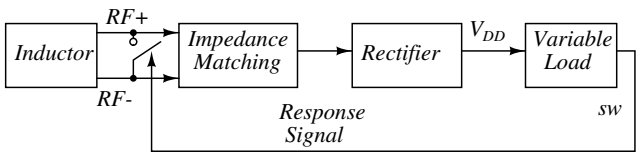


Fig. 2. Diagram of the integrated system.

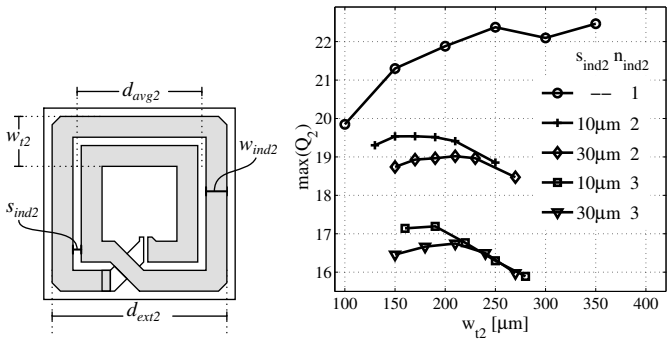
of efficiency and leads to a design independent from the primary inductor properties. So the optimization of the total efficiency is restricted to optimizing the values of Q_2, p and η_{RT}.

III. System Design

The system designed in this section is illustrated in Fig. 2. It is composed of a WPT receiver and a variable load. The energy is received by an integrated inductor occupying the outermost area of the chip. Following the inductor, a passive network provides conjugate matching between the link and rectifier impedance. Then, a rectifier converts the RF input signal to a DC voltage that powers a ring oscillator, which performs as a variable load. The oscillator is used to generate a signal that is sent back to the transmitter by the inductive link. The oscillator frequency carries the information about the power received by the WPT system.

A. Integrated Inductor

The integrated inductor was implemented in the uppermost metal level of an 180 nm RF-CMOS technology. The inductor design variables are the turns number n_{ind2}, the line width w_{ind2} and the turns separation s_{ind2}, as shown in Fig. 3(a). The external diameter (d_{ext2}) must be as large as possible to maximize the magnetic flux enclosed by the inductor, in this case that value is 1460 μm.



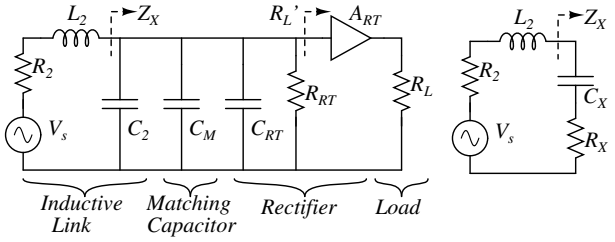
(a) (b)

Fig. 3. (a) Two-turns inductor. (b) Maximum Q_2 for several inductors.

In order to find the inductor dimensions that maximize its quality factor, we did electromagnetic simulations using the software EM-PRO from Agilent®, where the variables w_{t2} and s_{ind2} were swept for n_{ind2}=1,2 and 3. The maximum quality factor for each inductor is plotted in Fig. 3(b) as function of w_{t2}. According to the figure the inductor with n_{ind2}=1 and w_{ind2}=250 μm has the highest quality factor (Q_2=22.4), which happens when the link frequency is 1.04 GHz. As a consequence, this was the frequency chosen for operating the system.

B. Impedance matching network

Two factors were considered for choosing the matching network topology: (i) The network should not include inductors, because integrated inductors have poor quality factor. (ii) The network must be as simple as possible to reduce the sensitivity to process variability. After these assumptions, we decided for using a single matching capacitor (C_M), connected in parallel to the inductor.



(a) (b)

Fig. 4. Model for the power receiver: (a) Extended. (b) Simplified.

An electrical model to calculate the impedance matching is presented in Fig. 4(a), where C_2 models the self-resonance frequency of the inductor, C_{RT} is the input capacitance of the rectifier, R_{RT} represents the rectifier losses, A_{RT} is the voltage gain of the rectifier, and R_L is the load. The model of Fig. 4(a) can be simplified at the frequency of interest resulting in Fig. 4(b). The conditions for impedance matching are met by choosing the values of C_M and R_L so that C_X=1/($\omega^2 L_2$) and R_X=R_2, for a given rectifier.

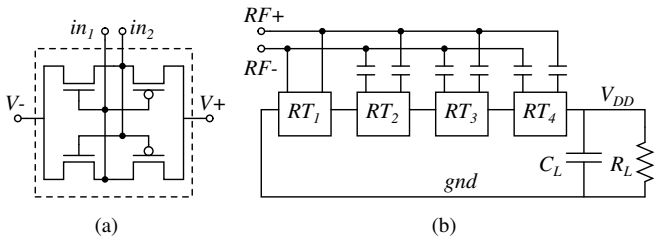
Using R_L to match the receiver means that there is a received power level that optimizes efficiency. A problem arises when the maximum efficiency occurs at a high level of power. There are two ways to move the optimal power to a lower value: (i) Increase A_{RT} by increasing the number of stages in the rectifier, because the equivalent resistance R_L' will decrease and the matching condition will occurs at a lower power level; (ii) increase the equivalent resistance of the inductor by reducing w_{ind2} or by increasing n_{ind2}, decreasing Q_2 and as a consequence, decreasing the total efficiency in both cases. Since the main objective in this design is to maximize the efficiency, we preferred to use an inductor with the best quality factor and keep the optimal power level at a moderated value (1 dBm) by implementing a four-stage rectifier.

The matching efficiency can be evaluated by inspecting the ratio between the input power at the rectifier P_{RT} and the available power from the inductor P_{avs}, defined as:

$$\eta_M = \frac{P_{RT}}{P_{avs}}. \tag{4}$$

C. Rectifier

The design of the rectifier considered the efficiency as the main figure of merit. The rectifier topology was based in [9] due to its high efficiency and simplicity and it is is shown in Fig. 5(a). The number of stages was chosen to be four, in order to have 2.5 V at the output when the available power is 1 dBm. The block diagram of the four-stages rectifier is shown in Fig. 5(b).



(a) (b)

Fig. 5. Rectifier: (a) CMOS schematic of each stage. (b) Block diagram.

All transistors in Fig. 5(a) have the minimal length (0.18 μm) and width W_M=30 μm, which corresponds to the best compromise

between η_M and η_{RT}. The NMOS transistors are triple-well devices, which permits to connect their sources to their body terminals. The rectifier efficiency was simulated as function of the available power from the inductive link (P_{avs}) for several values of R_L and the results are shown in Fig. 6(a). We observe in the figure that for each value of R_L there is a value of P_{avs} that maximizes the efficiency of the rectifier η_{RT}. We extracted the point of maximum of each curve in Fig. 6(a) and plotted them against P_{avs} into Fig. 6(b). The values of η_M and $\eta_M\eta_{RT}$ corresponding to the points extracted were plotted in Fig. 6(c) and in Fig. 6(d) respectively. Although the rectifier alone can have efficiencies greater than 60% for a wide rank of P_{avs} values, the highest $\eta_M.\eta_{RT}$ values are observed for P_{avs} between 0 and 2 dBm and R_L between 7 $k\Omega$ and 10 $k\Omega$. Outside of this band, total efficiency decreases due to impedance mismatch between the link and the rectifier. Post-layout simulations showed that the best impedance matching is obtained when P_{avs}=1 dBm and the load is R_L=10 $k\Omega$, resulting in V_{DD}=2.5 V.

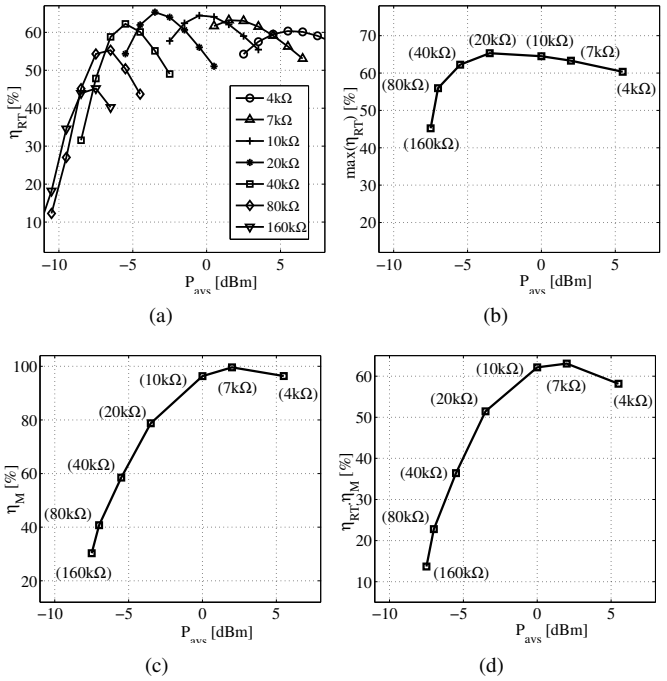


Fig. 6. (a) Rectifier efficiency for different R_L values. (b) Maximum η_{RT}. (c) Efficiency in power transferring due to impedance mismatch. (d) Matching and rectifier efficiency.

D. Variable Load and Response Generation

In order to measure the efficiency of the system, we designed a non-intrusive test strategy. Instead of a fixed resistance, we chose an oscillator as the load because it provides a value of R_L that is a function of the input power, while the output of the oscillator can activate a backscattering device. Thus, we can conclude that the oscillator is a variable load, dependent on the input power. In addition, by measuring the frequency of the envelop of the backscattered signal, we can estimate the power that is being received with no requirement of wires.

The variable load is based on a seven-stage ring oscillator whose frequency and current consumption vary with the supply voltage, as shown in Fig. 7(a). Following the ring oscillator, a flip-flop is employed to divide by two the oscillator frequency to ensure a 50% duty cycle for the sw signal. The schematic of the inverter used in the oscillator is shown in Fig. 7(b). In addition to the NMOS and PMOS transistors forming a conventional inverter, we added transistors with sources connected to the drains acting as capacitors to decrease the frequency of oscillation. We also added an 1 $M\Omega$ resistance in parallel with the PMOS transistor to allow the operation of the circuit at low V_{DD} values. So the designed circuit can operate for V_{DD} between 0.7 V and 3.6 V, as verified by simulations with typical-case models.

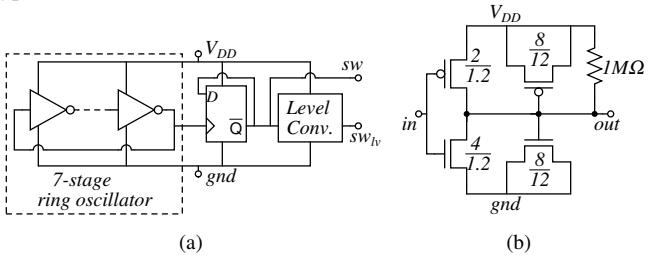


Fig. 7. Variable load: (a) Blocks diagram. (b) Inverter.

The frequency of the response signal (f_{sw}) can not be so high, because it will be band-pass filtered by the transmitter resonant tank. Simulations at system level done with ADS shows that f_{sw} must be lower than 10 MHz. On the other hand, low values of f_{sw} would require a large capacitor C_L according to (5):

$$C_L = \frac{V_{DD}}{4.R_L.f_{sw}.\Delta V}, \tag{5}$$

where ΔV is the variation of V_{DD} due to charging and discharging C_L at f_{sw} frequency. We chose ΔV=0.1 V and f_{sw}=3.5 MHz at the nominal value of V_{DD} (2.5 V), which leads to a value of C_L=180 pF.

When the switch at the terminals of the inductor is open (sw=0), by energy conservation, half of the current supplied by the rectifier goes to the variable load (R_V) and the other half charges the capacitor C_L, so the equivalent load R_L is $R_V/2$. The dimensions for transistors in Fig. 7b were chosen to adjust R_V=20 $k\Omega$ and f_{sw}=3.5 MHz for V_{DD}=2.5 V.

The switch used for load modulation is implemented as shown in Fig. 8. Two NMOS transistors (one for 1.8 V signal and the other for 3.3 V signal) are connected between the terminals of the inductor. Their lengths were kept at the respective minimum values for decreasing the ON resistance, while their widths were designed for keeping the ON-OFF amplitudes ratio (A_{ON}/A_{OFF}) higher than 10. Other transistors were used to tie down to ground the RF+ and RF-, aiming at decreasing the ON resistance of the main switches.

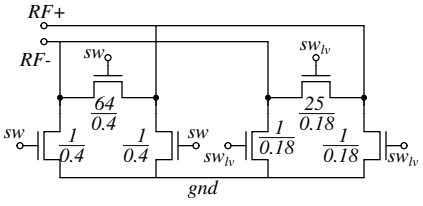


Fig. 8. Switch for load modulation.

IV. RESULTS

The layout of the system can be seen in Fig. 9. It occupies a silicon surface 1.5 $mm \times 1.5\ mm$. In addition to the receiving inductor and to the full system, an extra cell containing only the variable load was included for characterization purposes.

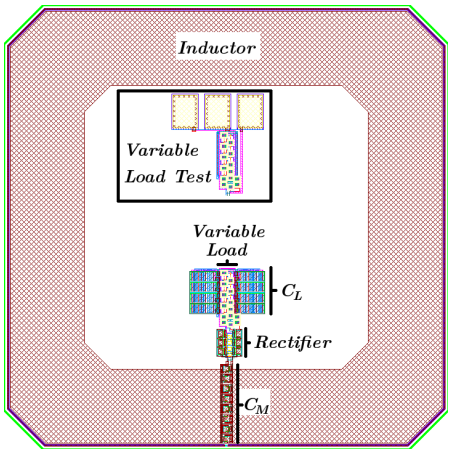


Fig. 9. Layout of the chip.

The complete system was simulated after layout parasitic extraction and the transient response is shown in Fig. 10. In this simulation, the power available at the inductor is 1 dBm and typical-case models for MOS transistors were used. The oscillator start-up is facilitated by the characteristic of its variable power consumption, which is low for low V_{DD} values. It takes approximately 5 μs for V_{DD} to reach the steady-state at 2.5 V. In steady state, V_{DD} suffers variations as expected due to the charging-discharging process of capacitor C_L at 3.5 MHz. We can see that the signal at the terminals of the inductor (RF+ e RF-) is correctly attenuated when sw is high, implying a correct backscattering.

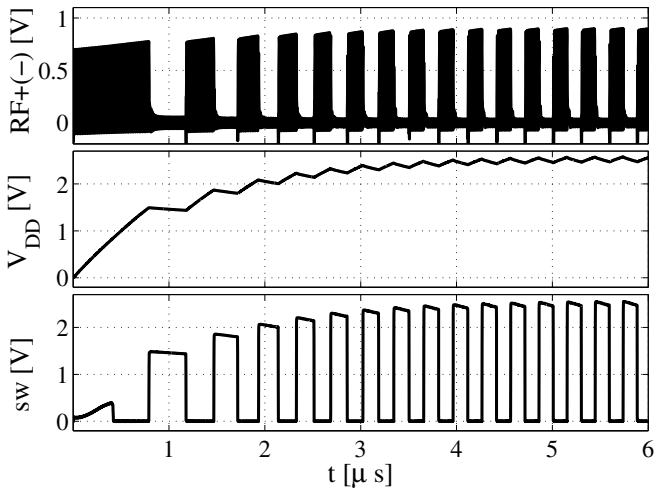


Fig. 10. Transient simulation of the receiver.

In order to verify the performance of the circuit, we did corner simulations and the results are summarized in Table I. The efficiency in the last column was calculated by measuring f_{sw} and associating it to the power consumed by R_V. That power value was multiplied by 2, because the rectifier only receives power half of the time. From the table we can conclude that the system can receive and respond correctly for P_{avs} between -7 dBm and 6 dBm.

V. Conclusion

In this paper we presented an integrated circuit designed to corroborate the feasibility of a wireless power transfer receiver, fully implemented in a constrained silicon area of 1.5 mm × 1.5 mm, even including the receiving inductor. By means of a backscattering device, the system responded to the level of the received power, allowing for the estimation of its total efficiency. In addition, a design methodology was applied in order to establish the trade-offs between the design variables, the resource restrictions and the highest efficiency. We found that the best inductor should have a single turn and its highest quality factor was reached around 1 GHz, keeping the possibility of powering implants at UHF frequencies. The combined efficiency of the matching network and the rectifier was 57%.

TABLE I
Corner simulations of the integrated system.

P_{avs} [dBm]	V_{DD} [V]	f_{sw} [MHz]	A_{ON} [V]	A_{OFF} [mV]	$\eta_M.\eta_{RT}$ [%]
Typical case					
-7	1.1	0.6	0.5	29	17
1	2.5	3.5	0.9	33	57
6	3.5	5.2	1.3	72	54
Fast case					
-7	1.2	1.1	0.5	22	28
1	2.4	3.9	0.9	34	59
6	3.3	5.7	1.2	60	54
Slow case					
-7	1.0	0.3	0.5	42	10
1	2.6	3.2	0.9	40	55
6	3.6	4.9	1.3	71	54

Acknowledgment

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